REMARKS

In the Office Action, the Examiner rejected claims 1, 11, 20-23 under 35 U.S.C. §102(b) as being anticipated by United States Patent 5,959,881 issued to Trimberger ("Trimberger"). The Examiner also rejected claims 3-7, 10, and 12-17 under 35 U.S.C. §103(a) as being unpatentable over Trimberger in view of United States Patent 6,134,705 issued to Pedersen et al. ("Pedersen"). Furthermore, the Examiner objected to claims 8-9 and 18-19 as being dependent upon a rejected based claim. However, the Examiner stated that claims 8-9 and 18-19 would be allowable if rewritten in independent form to include all of the limitations of the base claim and any intervening claims. Applicants have not amended or added any claims. Accordingly, claims 1 and 3-23 will be pending after entry of these Amendments.

I. Rejection to Claims 1, 3-7, 10, and 21-22

In the Office Action, the Examiner rejected claims 1 and 21-22 under §102(b) as being anticipated by Trimberger. The Examiner also rejected claims 3-7 and 10 under §103(a) as being unpatentable over Trimberger in view of Pedersen. Claims 3-7, 10, and 21-22 are directly or indirectly dependent on claim 1.

Claim 1 recites a computer-readable medium encoded with a data storage structure. The data storage structure stores a group of sub-networks. Each sub-network performs at least three output functions. The data storage structure stores each sub-network indexed by a parameter derived from all output functions of the sub-network.

Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest the data storage structure of claim 1 for at least the following four reasons. *First*, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a computer-readable medium encoded with a data storage structure. In the Office Action, the Examiner cited figure 3 and column 6, line 42 through column 7, line 28 of Trimberger to suggest such a

limitation. Furthermore, in the remarks to the previous Office Action Response submitted on 11/6/2006, the Examiner on page 12 of the current Office Action cited column 1, lines 19-43 of Trimberger, stating that the CLBs of figure 3 of Trimberger can be configured as routing structures as an array under the FPGA which includes data storage for the CLBs.

Rather than specify encoded software structures for data storage, the cited lines of Trimberger specify physical hardware components such as conventional look up tables and general purpose Random Access Memory (RAM) without disclosing any data structures encoded within such physical hardware components. *See*, Trimberger, column 6, lines 14-17 and 37-41. Therefore, Applicants respectfully submit that the cited physical circuit components of Trimberger disclose storage components as opposed to the data structures encoded within the computer-readable medium of claim 1.

Furthermore, in the remarks to the previous Office Action Response, the Examiner stated that "CLBs are configured as a routing structure as an array under FPGA which include data storage for the CLBs." Applicants respectfully submit that the remarks specify physical circuit components as opposed to the encoded software data structures of claim 1. Therefore, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a computer-readable medium encoded with a data storage structure.

Second, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a data storage structure for storing sub-networks. In the Office Action, the Examiner cited figure 3 and column 6, line 42 through column 7, line 28 of Trimberger to suggest such a limitation. Furthermore, in the remarks to the previous Office Action Response submitted on 11/6/2006, the Examiner on page 12 of the current Office Action cited column 1, lines 19-43 of Trimberger stating that the CLBs of figure 3 of Trimberger can be configured as routing structures as an array under the FPGA which includes data storage for the CLBs.

Applicants respectfully submit that the cited lines of Trimberger do not disclose, teach, or even suggest data storage structures for storing sub-networks. Instead, the cited lines specify storing "[t]hree types of data (implying three types of memory or storage)". *See*, Trimberger, column 5, lines 55-57. The stored data includes configuration data for configuring logic blocks, user data generated by logic, and state data for defining the logical values of nodes in the user logic, but not sub-networks. *See*, Trimberger, column 5, lines 55-57. Therefore, as should be evident from the above lines, Trimberger does not disclose or teach data storage structures for storing sub-networks.

Moreover, in response to the previous remarks submitted by the Applicants, the Examiner stated that the Trimberger CLBs can be configured as routing structures under the FPGA which includes data storage for the CLBs. Applicants respectfully submit that the Examiner has only identified storage elements for storing configuration data for the CLB and storage elements for storing generalized data. *See*, Trimberger, column 1, lines 19-43. The Examiner has not identified a data storage structure for storing sub-networks.

Third, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of anticipation, because Trimberger does not disclose every limitation of claim 1. For instance, claim 1 recites a data storage structure that stores each sub-network indexed by a parameter derived from all output functions of the sub-network. Rather than specify an index parameter derived from all output functions of the sub-network, the Examiner in his remarks to the previous Office Action Response cites figure 3, column 5, lines 59-67 and column 6, line 42 though column 7, line 28 alleging that Trimberger stores each sub-network based on a time index. Therefore, Applicants respectfully submit that Trimberger does not anticipate claim 1, because the method of claim 1 stores each sub-network based on an index derived from all output functions of the sub-network and the Examiner has cited to storage based on a time-index.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Furthermore, in page 13 of the current Office Action, the Examiner states that after having consulted with primary examiners from respective art units, it is suggested that references of prior art should be plenty. Applicants respectfully request that the Examiner produce such references to satisfy the Examiner's burden for establishing a prima facie rejection of claim 1.

Fourth, Applicants respectfully submit that even if a time index is derived from all output functions of the sub-network, Trimberger still does not disclose, teach, or even suggest a data storage structure that stores each sub-network indexed by a parameter derived from all output functions of the sub-network. In the Office Action, the Examiner cited figure 3, column 5, lines 59-67 and column 6, line 42 through column 7, line 28 of Trimberger to suggest such a limitation.

In the cited lines of Trimberger, the micro registers 324 and 325 of figure 3 of Trimberger are the storage elements for storing the alleged sub-networks. However, Applicants respectfully submit that nowhere within the cited lines or anywhere else within Trimberger is it disclosed that sub-networks are stored within the micro registers based on a time index. Instead, storage within the micro registers is explained in figure 3a of Trimberger. Figure 3a specifies register write select (RWS) signals for determining which micro register bit to write and Figure 3a clearly states that such RWS signals are not generated either by a time index of a sub-network or by output functions of a sub-network. *See*, Trimberger, column 7, lines 29-47. Therefore, Applicants respectfully submit that Trimberger does not disclose storing a sub-network within a data storage structure based on an index parameter derived from all the output functions of the sub-network.

In view of the foregoing remarks, Applicants respectfully submit that the cited references do not render claim 1 invalid. Given that claims 3-7, 10 and 21-22 are dependent on claim 1, Applicants respectfully submit that these claims be allowable over the cited reference for at least the same reasons that were provided above for claim 1. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 1, 3-7, 10, and 21-22.

II. Rejection to Claims 11-17, 20, and 23

In the Office Action, the Examiner rejected claims 11, 20 and 23 under §102(b) as being anticipated by Trimberger. The Examiner also rejected claims 12-17 under §103(a) as being unpatentable over Trimberger in view of Pedersen. Claims 12-17, 20, and 23 are directly or indirectly dependent on claim 11. Claim 11 recites a sub-network record management system that includes a data storage structure that stores a group of sub-networks. Each sub-network performs a set of output functions. The data storage structure stores each sub-network based on a parameter derived from the set of output functions of the sub-network. The parameter is used to retrieve the sub-network from the data storage structure. The sub-network record management system also includes a data access manager that identifies and retrieves sub-networks from the data storage structure.

Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest the sub-network management system of claim 11 for at least the following five reasons. *First*, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a sub-network record management system that has a data access manager that identifies and retrieves sub-networks from a data storage structure.

In the Office Action, the Examiner cited figure 3 and column 6, line 42 through column 7, line 28 for specifying such a data access manager, "where the flip-flops of the configurable logic block access and retrieve the outputs of functional generators." *See*, Office Action, page 6.

Figure 3 of Trimberger is a block diagram comprised of a pair of generic D-flip flops enabled via certain control signals fed by a pair of micro-registers which store the configuration data. Applicants respectfully submit that the flip-flops do not identify nor retrieve sub-networks from the data storage structure. Flip-flops are simple memory elements that store individual bits of data passed in from the input lines and do not disclose the identifying or retrieving of sub-networks. Therefore, Applicants respectfully submit that the Examiner has failed to identify how the cited figure and paragraphs teach, suggest, or disclose a sub-network record management system that has a data access manager that identifies and retrieves sub-networks from a data storage structure.

Second, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a computer-readable medium encoded with a data storage structure. In the Office Action, the Examiner cited figure 3 and column 6, line 42 through column 7, line 28 of Trimberger to suggest such a limitation. Furthermore, in the remarks to the previous Office Action Response submitted on 11/6/2006, the Examiner on page 12 of the current Office Action cited column 1, lines 19-43 of Trimberger, stating that the CLBs of figure 3 of Trimberger can be configured as routing structures as an array under the FPGA which includes data storage for the CLBs.

Rather than specify encoded software structures for data storage, the cited lines of Trimberger specify physical hardware components such as conventional look up tables and general purpose Random Access Memory (RAM) without disclosing any data structures encoded within such physical hardware components. *See*, Trimberger, column 6, lines 14-17 and 37-41. Therefore, Applicants respectfully submit that the cited physical circuit components of Trimberger disclose storage components as opposed to the data structures encoded within the computer-readable medium of claim 11.

Furthermore, in the remarks to the previous Office Action Response, the Examiner stated that "CLBs are configured as a routing structure as an array under FPGA which include data storage for the CLBs." Applicants respectfully submit that the remarks specify physical circuit components as opposed to the encoded software data structures of claim 11. Therefore, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a computer-readable medium encoded with a data storage structure.

Third, Applicants respectfully submit that Trimberger does not disclose, teach, or even suggest a data storage structure for storing sub-networks. In the Office Action, the Examiner cited figure 3 and column 6, line 42 through column 7, line 28 of Trimberger to suggest such a limitation. Furthermore, in the remarks to the previous Office Action Response submitted on 11/6/2006, the Examiner on page 12 of the current Office Action cited column 1, lines 19-43 of Trimberger stating that the CLBs of figure 3 of Trimberger can be configured as routing structures as an array under the FPGA which includes data storage for the CLBs.

Applicants respectfully submit that the cited lines of Trimberger do not disclose, teach, or even suggest data storage structures for storing sub-networks. Instead, the cited lines specify storing "[t]hree types of data (implying three types of memory or storage)". *See*, Trimberger, column 5, lines 55-57. The stored data includes configuration data for configuring logic blocks, user data generated by logic, and state data for defining the logical values of nodes in the user logic, but not sub-networks. *See*, Trimberger, column 5, lines 55-57. Therefore, as should be evident from the above lines, Trimberger does not disclose or teach data storage structures for storing sub-networks.

Moreover, in response to the previous remarks submitted by the Applicants, the Examiner stated that the Trimberger CLBs can be configured as routing structures under the FPGA which includes data storage for the CLBs. Applicants respectfully submit that the

Examiner has only identified storage elements for storing configuration data for the CLB and storage elements for storing generalized data. *See*, Trimberger, column 1, lines 19-43. The Examiner has not identified a data storage structure for storing sub-networks.

Fourth, Applicants respectfully submit that the Examiner has failed to establish a *prima facie* case of anticipation, because Trimberger does not disclose every limitation of claim 11. For instance, claim 11 recites a data storage structure that stores each sub-network indexed by a parameter derived from all output functions of the sub-network. Rather than specify an index parameter derived from all output functions of the sub-network, the Examiner in his remarks to the previous Office Action Response cites figure 3, column 5, lines 59-67 and column 6, line 42 though column 7, line 28 alleging that Trimberger stores each sub-network based on a time index. Therefore, Applicants respectfully submit that Trimberger does not anticipate claim 11, because the method of claim 11 stores each sub-network based on an index derived from all output functions of the sub-network and the Examiner has cited to storage based on a time-index. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Furthermore, in page 13 of the current Office Action, the Examiner states that after having consulted with primary examiners from respective art units, it is suggested that references of prior art should be plenty. Applicants respectfully request that the Examiner produce such references to satisfy the Examiner's burden for establishing a prima facie rejection of claim 11. Therefore, because the method of claim 11 stores each sub-network based on an index derived from all output functions of the sub-network, and because the Examiner has suggested storage based on a time-index, Applicants respectfully submit that Trimberger does not anticipate claim 11.

Fifth, Applicants respectfully submit that even if a time index is derived from all output functions of the sub-network, Trimberger still does not disclose, teach, or even suggest a data storage structure that stores each sub-network indexed by a parameter derived from all output functions of the sub-network. In the Office Action, the Examiner cited figure 3, column 5, lines 59-67 and column 6, line 42 through column 7, line 28 of Trimberger to suggest such a limitation.

In the cited lines of Trimberger, the micro registers 324 and 325 of figure 3 of Trimberger are the storage elements for storing the alleged sub-networks. However, Applicants respectfully submit that nowhere within the cited lines or anywhere else within Trimberger is it disclosed that sub-networks are stored within the micro registers based on a time index. Instead, storage within the micro registers is explained in figure 3a of Trimberger. Figure 3a specifies register write select (RWS) signals for determining which micro register bit to write and Figure 3a clearly states that such RWS signals are not generated either by a time index of a sub-network or by output functions of a sub-network. *See*, Trimberger, column 7, lines 29-47. Therefore, Applicants respectfully submit that Trimberger does not disclose storing a sub-network within a data storage structure based on an index parameter derived from all the output functions of the sub-network.

In view of the foregoing remarks, Applicants respectfully submit that the cited references do not render claim 11 invalid. Given that claims 12-17, 20, and 23 are dependent on claim 11, Applicants respectfully submit that these claims be allowable over the cited references for at least the same reasons that were provided above for claim 11. Accordingly, Applicants respectfully request reconsideration and withdrawal of the rejection of claims 11-17, 20, and 23.

III. Allowable Claims 8-9 and 18-19

In the Office Action, the Examiner objected to claims 8-9 and 18-19 as being dependent

upon a rejected base claim. The Examiner stated that claims 8-9 and 18-19 were otherwise allowable if rewritten in independent form. Applicants respectfully thank the Examiner for the allowance. However, Applicants respectfully have not rewritten any of these claims in independent form since Applicants respectfully believe that the rejected independent claims 1 and 11 are patentable over the cited references. In view of the foregoing, Applicants respectfully request reconsideration of allowable dependent claims 8-9 and 18-19.

CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 1 and 3-23 are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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Dated: 3/26/2007 /Mani Adeli/

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